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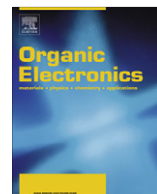
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Charge transport in high-performance ink-jet printed single-droplet organic transistors based on a silylethynyl substituted pentacene/insulating polymer blend

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ABSTRACT

We present a systematic study of the influence of material composition and ink-jet processing conditions on the charge transport in bottom-gate field-effect transistors based on blends of 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS-PEN) and polystyrene. After careful process optimizations of blending ratio and printing temperature we routinely can make transistors with an average mobility of 1 cm²/Vs (maximum value 1.5 cm²/Vs), on/off ratio exceeding 10⁷, and sharp turn-on in current (sub-threshold slopes approaching 60 mV/decade). These characteristics are superior to the TIPS-PEN only transistors. Using channel scaling measurements and scanning Kelvin probe microscopy, the sharp turn-on in current in the blends is attributed to a contact resistance that originates from a thin insulating layer between the injecting contacts and the semiconductor channel.

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1. Introduction

Mixing of two or more material components is a common industrial route to produce materials with tailor-made properties such as improved stiffness, impact strength, permeability, and/or electrical and optical properties. Polymer/polymer blends are commonly used as the active layer in organic solar cells [1,2]. Goffri et al. made organic transistors in which the active layer was a two-component blend based on polythiophenes and different insulating polymers [3]. This concept has also been applied successfully for small-molecule organic semiconductors such as 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS-PEN), blended with insulating or other semiconducting polymers [4,5].

Depending on the active materials, process conditions, and taking into account the thermodynamical driving force towards the most energetically favorable state and that most of the parent components in the blend are thermodynamically immiscible or partially-miscible, a vertical stratified morphology was achieved that leads to mobilities in field-effect transistors as high as the devices based on pure semiconductors, or even higher [5,6]. In most previous studies, blends were either spin-cast [7–9] or drop-cast [10,11]. High mobility (>1 cm²/Vs) transistors were reported only in the top-gate device geometry when spin-casting a small-molecule organic semiconductor blended with a semiconducting polymer [7,12–14]. These techniques require additional patterning steps after deposition if the transistors were to be integrated into circuits or display backplanes.

With drop-on-demand ink-jet printing the materials can be deposited locally, resulting in efficient material

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usage and a simpler process for device integration [15]. The challenge is to print well-defined structures from dilute inks. By blending the molecular semiconductor with a polymer, the viscosity of the printing solution can be varied. Blending, however, is also expected to impact the electrical performance of the final deposited transistor. This interplay is in fact the topic of this paper.

Two different approaches of ink-jet printing small-molecule semiconductors have been used: printing multiple droplets which coagulate into a film covering a relatively large area on the substrate, or single-droplet printing where each droplet forms an individual functional deposit. The former was adopted in a recent study by Madec et al. [16]. They ink-jet printed multiple droplets of inks containing TIPS-PEN and an amorphous and electrically insulating polymer, polystyrene (PS), at a blending ratio of 1/1 (w/w). By printing from a specific binary solvent mixture and/or using a multi-layer printing method, a continuous layer with improved morphology was achieved, and they found an increased mobility of up to $10^{-2} \text{ cm}^2/\text{Vs}$ (± 71 –80% variance) in bottom-gate/top-contact transistors. These mobilities are however much lower than the values of $0.12 \text{ cm}^2/\text{Vs}$ reported by Lim et al. [17] for single-droplet printing of pure TIPS-PEN from a solvent mixture, making it thus far unclear if blending with an insulating polymer can result in a further improvement in high-performance ink-jet printed transistors.

In this paper, we investigate single-droplet ink-jet printing of TIPS-PEN/PS blends, with each printed single droplet being an individual transistor [6,18]. This eliminates the need for additional patterning steps. As in the previous work of Lim [17], we use a bottom-gate/bottom-contact device geometry. This device architecture offers a straightforward route for downscaling of the transistor channel length to a few micrometers. In contrast to Lim's work, we did not rely on the unusual concentric ring arrangement of source and drain electrodes, because that configuration does not allow simple device integration. Here, we use conventional interdigitated comb structure for the source and drain electrodes.

To gain insight into the charge-transport properties of our devices, we study the differences between the transistors based on pure TIPS-PEN and TIPS-PEN/PS blends with respect to macroscopic device operation and local charge-transport properties, by using channel scaling studies and surface potential profilometry, respectively, and relate them to the morphology of the devices. The fundamental understanding of device operation obtained for our blend transistors provides valuable guidelines to the development of next generation transistors based on small-molecule semiconductor and insulating polymer blends.

2. Experimental

6,13-Bis(triisopropyl-silyl)ethynyl)pentacene (TIPS-PEN) was synthesized according to literature [19]. Polystyrene (PS), Mw = 9.58 kDa (Mn = 9.32 kDa, PDI = 1.03), was purchased from Fluka. 1,2,3,4-tetrahydronaphthalene (tetralin, purchased from Merck) was used as the solvent.

An ink-jet printing setup with a high-precision vertical translation stage and a Microfab glass nozzle (type MJ-ATP-01-50-DLC, 50 μm orifice diameter) was used to

print inks with a constant TIPS-PEN concentration of 20 mg/ml and varied PS concentrations according to their blending weight ratios. Each droplet with a typical volume of 50 pL was jetted on demand and aligned to the transistor channel region to form an individual device, on substrates that were kept at 70 or 20 °C. All printing experiments were performed in ambient cleanroom conditions.

Bottom-contact/bottom-gate transistors were printed on Si (n++)/SiO₂ substrates with an oxide thickness of 140 nm and photolithographically patterned Au as source and drain electrodes. A pentafluorobenzenethiol monolayer was deposited on Au electrodes [20]. The SiO₂ was treated with trichlorophenylsilane. The transistor channel length was varied between 2 and 40 μm . Device characteristics were measured at room temperature in inert atmosphere using an Agilent 4155C semiconductor parameter analyser. The field-effect mobilities of our transistors in linear (μ_{lin}) and saturation (μ_{sat}) regime were calculated from the two equations as follows, with $V_{DS} = -1 \text{ V}$ and -10 V , respectively [21]:

$$\mu_{lin}(V_G) = \frac{L}{W \cdot C_i} \frac{1}{V_{DS}} \left(\frac{\partial I_{SD}}{\partial V_G} \right) \quad (1)$$

$$\mu_{sat}(V_G) = \frac{2L}{W \cdot C_i} \left(\frac{\partial \sqrt{I_{SD}(V_G)}}{\partial V_G} \right)^2 \quad (2)$$

where C_i is the capacitance per unit area of the gate dielectric layer, and L and W are channel length and width, respectively. The threshold voltage (V_{th}) of our devices is extracted by extrapolating the square root (SQRT) of $|I_{SD,sat}|$ vs. V_G plot to $I_{SD,sat} = 0$ (as depicted in the plots in Fig. 1a). The sub-threshold slope (SS) value was calculated from the measured I_{SD} values over more than two decades above noise level, using the following equation:

$$SS = \frac{V_{G1} - V_{G2}}{\log_{10} \left(\frac{I_{SD1}}{I_{SD2}} \right)} \quad (3)$$

Optical micrographs were taken on a Leica DM2500M Microscope with cross-polarizers. SKPM was performed using a Veeco Dimension 3100 with a NanoScope IVa controller operating in the lift mode. For the comparison of contact resistance in the pure and blend transistors, a maximized scan size of $80 \times 80 \mu\text{m}^2$ was used here to span over three active channels in the transistors to rule out any local effects. To avoid any effect of morphological anisotropy due to the direction of crystal growth from periphery towards centre of the droplets, the scanning regions of SKPM on two groups of devices (pure vs. blend) were chosen at the same location relative to the exact centre of the droplets, and with the same scanning direction with respect to the orientation of interdigitated electrodes of the devices. First, the height profile was recorded with tapping-mode atomic force microscopy (AFM). In the second pass the tip is lifted at a fixed height of 50 nm above the surface, and a voltage is applied to the tip, to record the local surface potentials. Several effects can influence the accuracy of SKPM measurements, e.g. the distance between SKPM tip and the sample surface, the geometry of the tip and cantilever, and the relative in-plane positioning of the cantilever with respect to the interdigitated electrodes of transistors

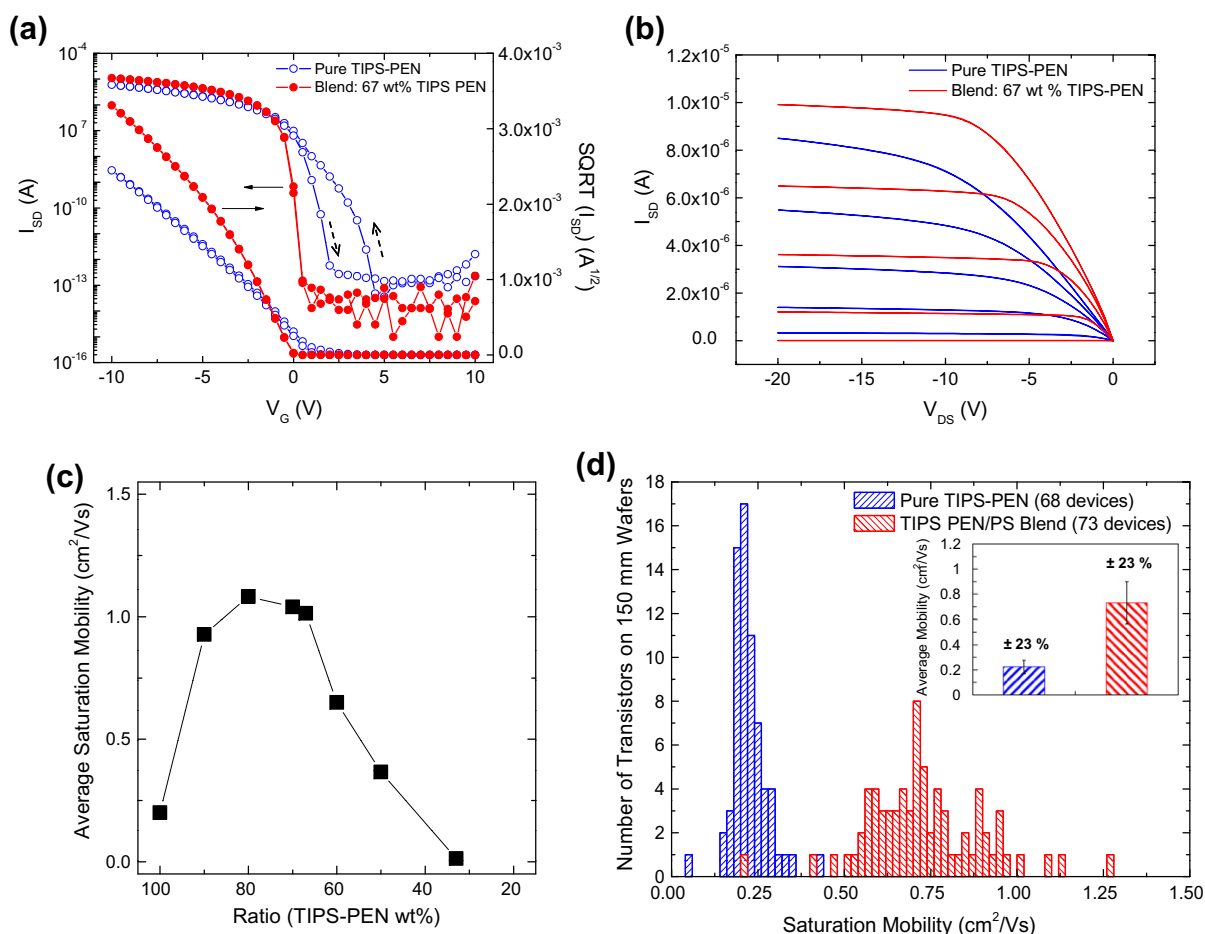


Fig. 1. (a) Transfer characteristics in saturation regime ($V_{DS} = -10$ V) for two representative transistors with pure TIPS-PEN channel (open circles in blue) and blend channel of 67 wt.% TIPS-PEN and 33 wt.% PS (solid circles in red). Channel length and width are 10 and 200 μm , respectively. The two dashed arrows indicate the counter-clockwise hysteresis for the pure device (gate swept from $+10$ V \rightarrow -10 V \rightarrow $+10$ V). The plot of the square root (SQRT) of I_{SD} vs. V_G was used to extract mobility as well as the threshold voltage (V_{th}): the blend device shows a mobility of 1.04 cm^2/Vs and a near-zero V_{th} , while the pure one has a mobility of 0.29 cm^2/Vs and a V_{th} of 2.5 V. (b) Output characteristics of the same two transistors as shown in (a). V_G was varied between 0 and -10 V at a step of -2.5 V. (c) Average saturation mobilities as a function of TIPS-PEN weight ratios in TIPS-PEN/PS blend transistors (averaged from >10 devices for each ratio). All devices were printed on 15 mm \times 15 mm square substrates at 70 $^\circ\text{C}$. (d) Histograms of saturation mobilities for 68 pure TIPS-PEN transistors and 73 blend (67 wt.% TIPS-PEN) transistors printed on 150 mm wafers. The inset shows their average mobility values. The relative variance (standard deviation divided by the average value) is 23% for pure TIPS-PEN as well as the blend devices. Transistors were printed at 70 $^\circ\text{C}$. Channel length and width are 5 and 1400 μm , respectively. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

[22–24]. The accuracy of our SKPM measurements is comparable to earlier reports on working organic transistors [22,25,26], with observed voltage drop from source to drain electrodes slightly lower than the actual bias applied (V_{DS}). Here we tend to attribute this smaller measured potential drops to the effect of non-local coupling between the entire cantilever/tip and the microscopic device surface, and/or a relatively high tip-sample distance of 50 nm in our measurements [23,24,27,28].

3. Results and discussion

3.1. Effect of insulating polymer (PS) on transistor device performance

Our transistors were independently processed over a period of 14 months on substrates that were prepared

under identical conditions. Over time no significant drift in transistor parameters was observed. Representative transfer characteristics in saturation ($V_{DS} = -10$ V) for pure TIPS-PEN transistors printed at 70 $^\circ\text{C}$ are shown in Fig. 1a (open circles in blue). Non-ideal sub-threshold behavior was observed in the form of ‘shoulder-like’ I_{SD} , with an obvious hysteresis between the forward and backward sweeps. This phenomenon was also reported by Lee et al. [29]. The average saturation mobility of pure TIPS-PEN transistors is 0.20 cm^2/Vs , comparable with earlier reports of ink-jet printing pure TIPS-PEN [6,17]. Adding a polymer binder to the pure TIPS-PEN ink dramatically improves the device characteristics (solid circles in red, Fig. 1a): the transistors switch on sharply at ~ 0 V, the on-current and mobility are higher than the pure TIPS-PEN devices and no hysteresis is observed. The sharp turn-on is a desirable device property for a switching transistor as it allows

high-speed and low-power operation. Typical output characteristics for pure TIPS-PEN and blend (67% TIPS-PEN) transistors are compared in Fig. 1b. No notable non-linearity of I_{SD} is observed for the pure or blend transistor; not even when the output characteristics are plotted in the form of $\Delta I_{SD}/\Delta V_{DS}$ vs. V_{DS} (graphs not shown). Next, we found that the device mobility is a function of relative weight ratio of TIPS-PEN/PS (Fig. 1c). For blends with 90–67 wt.% of TIPS-PEN, the average mobility has increased up to $\sim 1 \text{ cm}^2/\text{Vs}$, a factor of 5 higher than the pure TIPS-PEN ($0.20 \text{ cm}^2/\text{Vs}$). At lower concentration of TIPS-PEN (e.g. 60 wt.%) the mobility decreases. The average value and standard deviation of mobility (μ) in linear and saturation regime, on-current (I_{on}), and on/off ratio (I_{on}/I_{off}) for transistors (channel length: $10 \mu\text{m}$, on $15 \text{ mm} \times 15 \text{ mm}$ square substrates) printed at 70°C with different blending ratios are summarized in Table 1. At a processing temperature of 20°C we obtain typically lower device performance (Table 2). To further study large area uniformity, we printed 68 pure TIPS-PEN and 73 blend (67 wt.% TIPS-PEN) transistors with a channel length of $5 \mu\text{m}$ on 150 mm diameter wafers at 70°C . The histograms in Fig. 1d clearly demonstrate enhanced mobilities of our blend transistors over the entire wafer, with the relative variance (standard deviation divided by the average value) at the same level as the pure TIPS-PEN devices ($\pm 23\%$ in the inset of Fig. 1d). This demonstrates the potential of our blend inks for applications in large-area and low-cost organic electronics.

The observation that the mobility is increased by the presence of an insulator up to a critical blending ratio demonstrates that introducing an insulating polymer does not negatively affect the charge transporting layer in the device. This implies that in particular the composition and morphology of the first few nanometers of our TIPS-PEN/PS blend are similar to that of pure TIPS-PEN, as charge transport takes place at this zone in the semiconductor layer [30]. Similar behavior was recently reported for spin-cast blends of TIPS-PEN with poly(α -methylstyrene) [8,9], and blends of TIPS-PEN or fluorinated 5,11-bis(triethylsilyl)ethynyl anthradithiophene (diF TES-ADT) with a semiconducting polymer, polytriarylamine [7,12]. The results were explained by the occurrence of vertical stratification upon casting and solvent evaporation. During solvent drying TIPS-PEN is predominantly expelled to both top and bottom interfaces of the deposited films [8,9,12]. As long as phase separation leads to almost pure phase of

Table 2

Summary of transistor parameters for TIPS-PEN/PS transistors with different blending ratios printed on $15 \text{ mm} \times 15 \text{ mm}$ square substrates at 20°C , under the same processing conditions. Field-effect mobilities were extracted in linear (μ_{lin}) and saturation (μ_{sat}) regime, on-current (I_{on}) was measured at $V_G = -10 \text{ V}$, with $V_{DS} = -10 \text{ V}$. Data was obtained for >10 transistors of each ratio.

Ratio (TIPS-PEN wt.%)	$\mu_{lin} (\text{cm}^2/\text{Vs})$	$\mu_{sat} (\text{cm}^2/\text{Vs})$	$I_{on} (\mu\text{A})$
100	0.17 ± 0.03	0.15 ± 0.05	4.4 ± 0.9
67	0.53 ± 0.13	0.55 ± 0.14	7.8 ± 1.7
50	0.58 ± 0.47	0.65 ± 0.51	8.3 ± 6.6
33	0.02 ± 0.02	0.04 ± 0.04	0.3 ± 0.3

TIPS-PEN at the two interfaces, it should be possible to realize transistors with good performance. This hypothesis can explain why the mobility decreases at too high weight fraction of the polymer in our blends: phase separation is incomplete and no continuous film of TIPS-PEN is formed at the bottom interface of our devices. It can however not explain why the maximum mobility of the blends is higher than that of the pure TIPS-PEN transistors. At least two explanations have been proposed for the improved charge transport in the blend transistors. Ohe et al. suggested that the addition of polymer binder leads to slower drying and hence to a different morphology of the TIPS-PEN film [9]. Yoon et al. proposed that the polymer binder influences the film formation process of the small-molecule organic semiconductors and acts indirectly as a purification method [31].

Typical optical micrographs (cross-polarized reflection mode) in Fig. 2a present the morphology evolution of TIPS-PEN/PS blends printed at 70°C , with TIPS-PEN weight ratios ranging from 100% to 50%. Pure TIPS-PEN devices have irregular shaped crystalline deposit attributed to the de-pinning of the contact line during solvent drying (image of 100 wt.%), leading to limited crystal coverage on transistor channels. The addition of PS up to $\sim 40\%$ gives circular deposits with large crystals of TIPS-PEN that cover the whole device area with an improved crystal morphology (images of 80 and 67 wt.% of TIPS-PEN). Devices with this type of morphology have high mobility. At further higher concentration of PS, small and isolated TIPS-PEN crystals in a matrix of amorphous materials are observed (images of 50 wt.%). The lack of crystalline TIPS-PEN in this deposit explains the lower transistor performance and large parameter spread (Table 1). Corresponding transfer characteristics for the four transistors of Fig. 2a are compared in

Table 1

Summary of transistor parameters for TIPS-PEN/PS transistors with different blending ratios printed on $15 \text{ mm} \times 15 \text{ mm}$ square substrates at 70°C , under the same processing conditions. Field-effect mobilities were extracted in linear (μ_{lin}) and saturation (μ_{sat}) regime, on-current (I_{on}) and off-current were measured at $V_G = -10 \text{ V}$ and $+10 \text{ V}$, respectively, with $V_{DS} = -10 \text{ V}$. Data was obtained for >10 transistors of each ratio.

Ratio (TIPS-PEN wt.%)	$\mu_{lin} (\text{cm}^2/\text{Vs})$	$\mu_{sat} (\text{cm}^2/\text{Vs})$	$I_{on} (\mu\text{A})$	On/off ratio
100	0.23 ± 0.06	0.20 ± 0.07	4.5 ± 1.1	$4.9 \times 10^6 \pm 3.0 \times 10^6$
90	0.72 ± 0.14	0.93 ± 0.23	8.6 ± 1.7	$1.2 \times 10^7 \pm 1.0 \times 10^7$
80	0.90 ± 0.14	1.08 ± 0.16	9.4 ± 1.7	$3.0 \times 10^7 \pm 1.8 \times 10^7$
70	0.83 ± 0.22	1.04 ± 0.26	9.7 ± 2.8	$2.9 \times 10^7 \pm 1.7 \times 10^7$
67	0.85 ± 0.09	1.01 ± 0.12	10.8 ± 1.3	$4.9 \times 10^7 \pm 2.3 \times 10^7$
60	0.53 ± 0.24	0.66 ± 0.30	5.7 ± 2.5	$3.8 \times 10^7 \pm 6.6 \times 10^7$
50	0.30 ± 0.27	0.37 ± 0.33	3.6 ± 3.4	$2.2 \times 10^7 \pm 3.1 \times 10^7$
33	0.005 ± 0.003	0.01 ± 0.009	0.06 ± 0.04	$2.1 \times 10^5 \pm 1.6 \times 10^5$

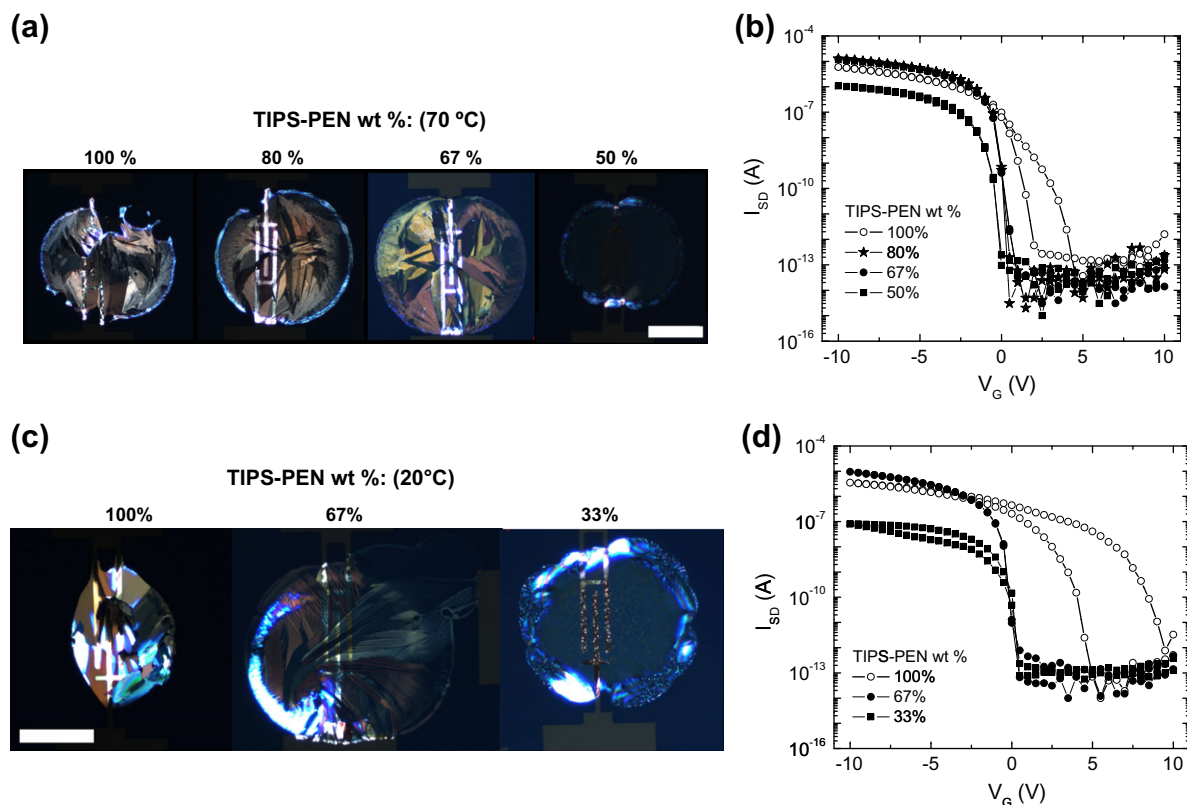


Fig. 2. (a) Representative cross-polarized optical micrographs showing the morphology transition of TIPS-PEN/PS blends with different TIPS-PEN concentrations printed at 70 °C. The scale bar indicates 100 μm . (b) Transfer characteristics in saturation regime ($V_{DS} = -10\text{ V}$) for transistors corresponding to the optical micrographs in (a). (c) Representative cross-polarized optical micrographs showing the morphology transition of TIPS-PEN/PS blends printed at 20 °C with decreased TIPS-PEN weight ratio from 100% to 33%. The scale bar indicates 100 μm . (d) Transfer characteristics in saturation regime ($V_{DS} = -10\text{ V}$) for the three transistors corresponding to the optical micrographs in (c).

Fig. 2b. Similar trends in contact-line pinning, transition of crystal morphology, and transistor performance as a function of polymer content were also observed when printing at a lower substrate temperature of 20 °C (Fig. 2c and d). The de-pinning effect, however, is more dominant for 20 °C: the lack of positioning control with ill-defined crystal coverage on transistor channels results in their lower device performance and larger spread (Table 2).

3.2. Channel scaling studies

In relation to the phase separation mentioned above, the steep on-switch of current (I_{SD}) of the blend devices is also informative. Steep sub-threshold slopes are observed for all blend transistors, i.e. independent of the TIPS-PEN/PS ratios and process temperatures. Steep sub-threshold slope and low threshold voltage (V_{th}) are usually taken as evidence of a high quality gate dielectric–semiconductor interface with few charge trapping centers [32,33]. This suggests that the polymer binder modifies the interface either directly, for instance, by forming a very thin wetting layer between the silane-treated dielectric and the molecular semiconductor, or indirectly, by influencing the molecular packing of the semiconductor leading to fewer grain boundaries. Meanwhile, reduced charging

effects at the top surface of the semiconductor channel ('backchannel effect') by the passivation/encapsulation of phase-separated insulating polymer can also explain the improved characteristics [29]. Although these explanations can play a role also in our blend devices, we propose a third explanation below.

The sub-threshold slope in most blend transistors is very close to the theoretical minimum of 60 mV/decade ($= kT/q \times \ln 10$) for an Ohmic charge injection from a metal into a semiconductor at room temperature [34,35]. Fig. 3 shows a representative sub-threshold slope as steep as 67 mV/decade in saturation regime for a blend transistor, calculated over more than 2 decades of I_{SD} . This points towards the existence of a tunneling barrier at the metal contacts, which is characterized by a highly non-linear I – V behavior in transfer characteristics [35–38].

We measured the channel length (L) dependence of the total resistance ($R_t = V_{DS}/I_{SD}$) at different gate biases (V_G) in linear regime ($V_{DS} = -1\text{ V}$) for two groups of transistors: pure TIPS-PEN vs. blend (67 wt.% TIPS-PEN) (Fig. 4). For the sake of comparison we choose the device series to have similar extracted mobilities. This implies that this group of blend transistors has below-average mobilities. As compared in Fig. 4, R_t decreases linearly with L for the pure transistors, down to a channel length of 2 μm . In contrast,

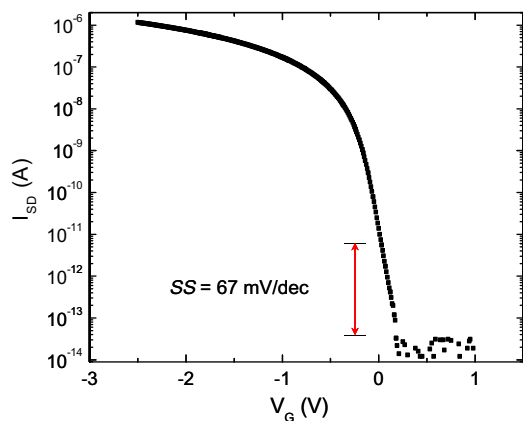


Fig. 3. A representative TIPS-PEN/PS blend (67 wt.% TIPS-PEN) transistor showing the extremely steep sub-threshold slope (SS) of 67 mV/decade in saturation regime ($V_{DS} = -10$ V). The SS value was calculated from the measured I_{SD} values over more than two decades above noise level, as indicated by the red arrows. The I - V curve was measured with 0.01 V increment per step of V_G . (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

for the blend transistors, R_t does not decrease further if we decrease L below 10 μm , illustrating the importance of a parasitic contact resistance, R_{sd} , in series with the channel resistance. Apparently the influence of R_{sd} for the extraction of intrinsic channel mobility is substantial for the blend but relatively small for the pure TIPS-PEN transistors. From similar analysis for other blend device series, we know that in all cases the blend transistors are influenced by contact resistance (contact limited) and that the variation in R_{sd} is one of the major causes for the variation in mobility reported in Table 1. This makes it particularly relevant to study the origin of the parasitic contact resistance.

3.3. Contact resistance identified by SKPM

To study the origin of parasitic contact resistance in our devices and correlate it to local charge-transport properties, scanning Kelvin probe microscopy (SKPM) measurements were performed during device operation [39]. As

shown in the potential image of Fig. 5a, the pure TIPS-PEN transistors show typical parabolic potential profiles from source to drain electrodes when devices were operated in saturation regime, with a small voltage drop at the source electrode, <15% relative to the voltage drop across the channel. Some negligible potential steps along the channel can be discerned and attributed to the grain boundary effects (see corresponding topography image in Fig. 5a), in line with previous studies [25]. In contrast, the potential profiles of the blend (67 wt.% TIPS-PEN) transistors show significant voltage drops at the electrodes (Fig. 5b). Because >80% of the voltage drastically drops at the source electrodes, the profile inside the channel is absent of details.

This high-Ohmic spatial zone close to the source electrodes of blend devices suggests a substantial barrier for charge injection from the contacts into the channels. Based on the potential profiles in Fig. 5, we can quantitatively compare the contact resistance (R_{sd}) for pure and blend devices operated at the 'on-state' (bias conditions: $V_{DS} = -10$ V and $V_G = -10$ V [22,40]) using [22,39]:

$$R_{sd} = \frac{\Delta V_S + \Delta V_D}{I_{on}} \quad (4)$$

where ΔV_S and ΔV_D are the voltages drops at the source and drain electrodes (in Fig. 5), respectively, and I_{on} is the measured 'on-state' source-drain current I_{SD} . With such calculations we found R_{sd} for pure (~ 0.13 M Ω) and blend (~ 0.51 M Ω) devices, respectively, much higher in the blend.

3.4. Charge-trapping at the edges of Au electrodes in blend transistors

Recently electric force microscopy (EFM) was adopted to study charge trapping in TIPS-PEN transistors by Jaquith et al. [41]. Clear evidence of long-lived charge trapping was observed. In their study the films were prepared using different processing conditions, leading to different mobilities (10^{-4} – 10^{-3} cm²/Vs). In that work frequency-shift EFM images were recorded to reflect the variations in local trap density. Here, we use SKPM to directly monitor the possi-

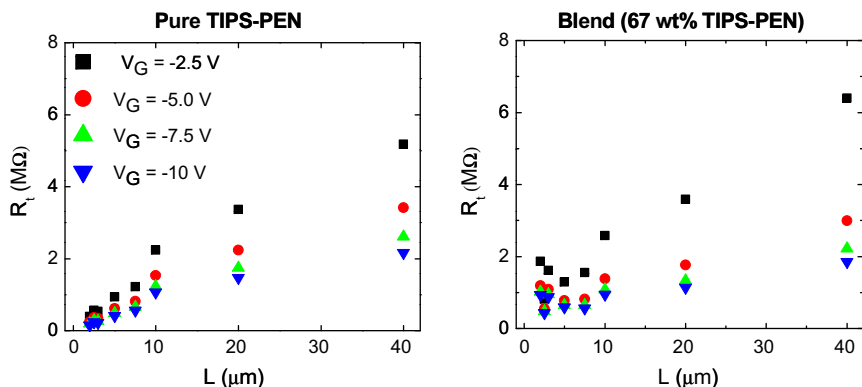


Fig. 4. Channel length dependence of total resistance (R_t) in linear regime ($V_{DS} = -1$ V) at different gate biases (V_G) for pure TIPS-PEN and blend (67 wt.% TIPS-PEN) transistors.

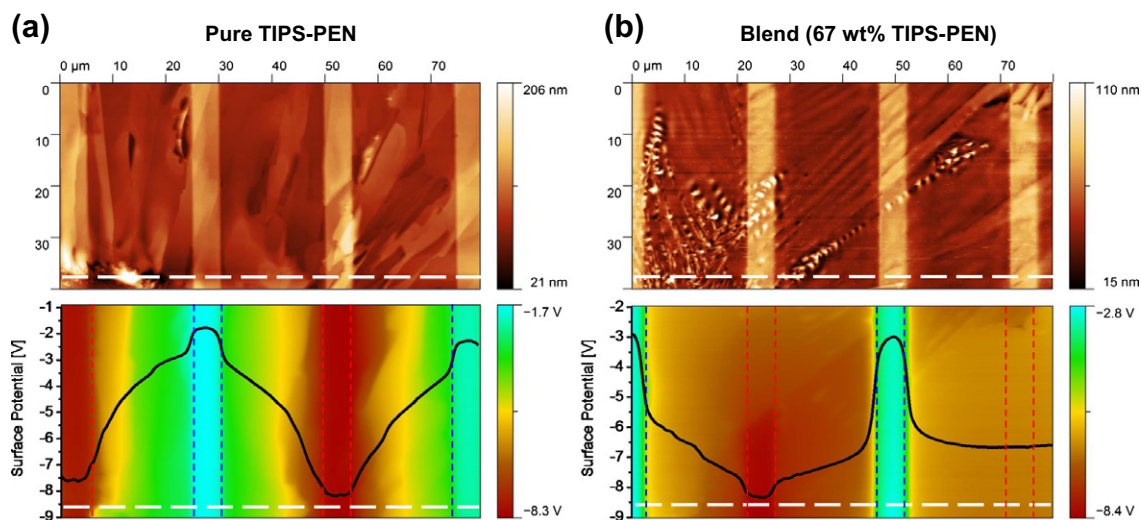


Fig. 5. 2D topography and corresponding surface potential images measured with SKPM of pure TIPS-PEN (a) and blend (67 wt.% TIPS-PEN) transistors (b), as shown in the upper and lower panels, respectively. White dashed lines indicate the positions where the potential cross-sections were taken. Solid black lines denote the cross-section potential profiles along the positions indicated by the dashed white lines. In the potential images, parallel dotted lines in the vertical direction indicate the positions of the edges of source (in blue) and drain (in red) electrodes. Channel length is 20 μm . The transistors were biased in saturation regime ($V_{DS} = -10$ V and $V_G = -10$ V). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

bly trapped charges by measuring their local surface potentials with time. To (possibly) create long-lived trapped charges in our samples, a gate bias of $V_G = -10$ V was applied for ~ 10 min. During this time, some of the mobile charges may become trapped. The biases were then set to zero in order to extract the mobile charges from the transistor channel, and the local electrostatic potential was measured immediately. Recorded potential images of a pure TIPS-PEN and a blend (67 wt.% TIPS-PEN) transistor are compared. As shown in Fig. 6a (middle image: $t = 0$), only few spots with slightly higher potentials are identified in pure TIPS-PEN channels. These can be correlated to grain boundaries or material voids from the corresponding topography image. The potential differences at these spots disappear on a time scale of ~ 1 h (bottom image in Fig. 6a: $t = 68$ min). In comparison, in the blend device we observed noticeable local surface potential variations (middle image in Fig. 6b: $t = 0$). If we attribute the contrast in these potential images to trapped positive charges (holes), then we observe substantial hole trapping at the edges of Au electrodes in the blend devices. These trapped holes in the blend films are very long-lived (bottom image in Fig. 6b: $t = 612$ min). For more than 10 h we observed no significant decrease of trapped charges as evidenced by the essentially unchanged potential image.

It has recently been shown that insulating polymer such as poly(α -methylstyrene) can trap charges (holes) in pentacene-based organic transistors [42], and these holes remain trapped in the insulating polymer until sufficient counter charges (electrons) can tunnel into the polymer from the channel [43]. Based on the clear differences of trapped charges in terms of locations, areal densities and life-times between our pure TIPS-PEN and blend devices, we argue that the hole trapping in our blend films is related to the local presence of insulating polymer (PS). The

potential variations in the blend films (Fig. 6b) are explained by a lateral phase-separation between TIPS-PEN enriched crystal grains and PS enriched regions. In particular, our SKPM results reveal obvious hole trapping effects exactly at the edges of the source/drain Au electrodes with no apparent correlation with its local crystal morphology. This strongly suggests the presence of a thin film of PS (or PS enriched phase) at the Au electrodes. Such an insulating barrier can explain the differences in sub-threshold slope of the I - V characteristics, contact resistance observed in channel scaling measurements, potential drops and hole trapping at the electrodes observed by SKPM, between our pure TIPS-PEN and blend devices.

3.5. Discussion on the relation between charge-trapping, threshold voltage and channel conductivity

If charges are trapped (de-trapped), or fixed space charges are distributed in the transistor channel on a time-scale comparable to the typical duration of the I - V measurement, it can be observed as a hysteresis during the forward and backward sweeps in transfer characteristics. We typically swept the voltages at a rate of 1 V/s, meaning a total measurement time of ~ 1 min.

In the case of pure TIPS-PEN transistors, non-ideal sub-threshold behavior was observed in the form of 'shoulder-like' I_{SD} , with an obvious hysteresis during gate sweeps (Fig. 1a). The (counter-clockwise) hysteresis was independent of the sweep direction, i.e. it was the same when sweeping the gate biases (V_G) in the opposite direction (from -10 V $\rightarrow +10$ V $\rightarrow -10$ V, graphs not shown). This hysteresis occurs in the depletion regime, i.e. when the bulk of the semiconductor is (partly) depleted of unintentional charges. We attribute it to charging effects at the top surface of the semiconductor channel (the so-called 'backchannel effect'),

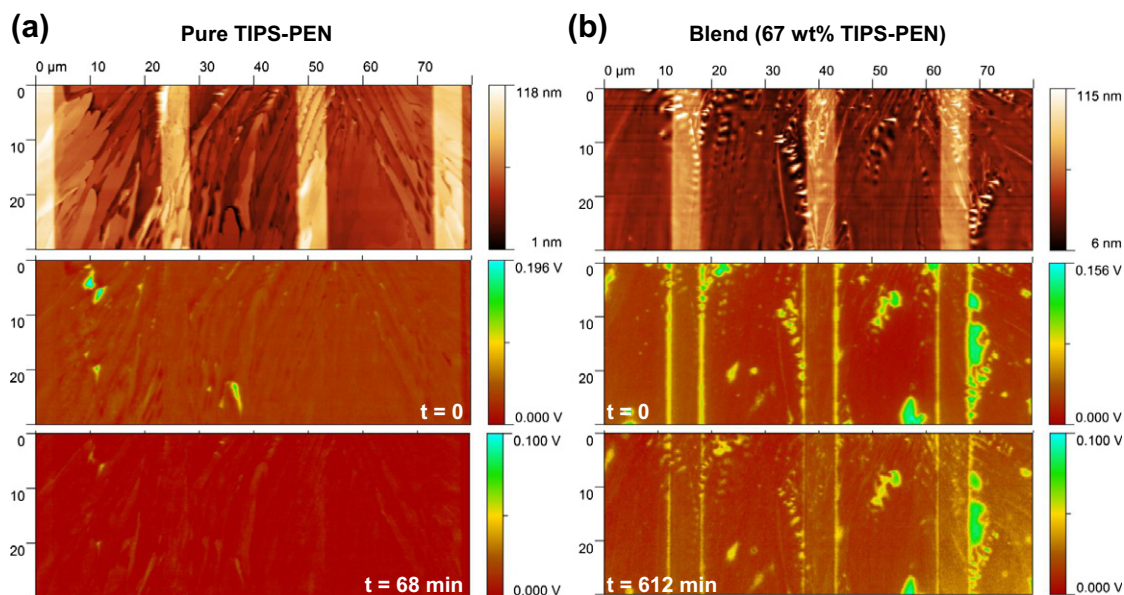


Fig. 6. Time-dependent surface potential images and corresponding 2D topographies recorded by SKPM, for pure TIPS-PEN (a) and blend (67 wt% TIPS-PEN) transistors (b). The potential images in the middle row ($t = 0$) were measured by grounding all electrodes immediately after a gate bias of -10 V was applied for 10 min. The potential images at the bottom row were measured at $t = 68$ and 612 min after three electrodes were grounded for the pure and blend device, respectively.

as previously reported by Lee et al. [29]. The transfer characteristics of our blend transistors (with different TIPS-PEN/PS ratios) are essentially hysteresis-free, independent of the direction or range of the gate sweeps. Apparently, the ‘back-channel effect’ is absent in these blend devices. This points to an additional advantage of the insulating polymer binder. It passivates the charge transport layer.

Trapped channel charges can result in shifts of transistor threshold voltages. Furthermore, deep and shallow trapping can also influence the charge transport negatively. We found that in our blend devices that (1) the existence of insulating polymer causes long-term trapping of holes, and (2) the existence of insulating polymer increases the field-effect mobility and has only a marginal influence on the threshold voltage. We attribute this seeming contradiction to the fact that charge-trapping takes place almost exclusively at the contact edges and to a far lesser extent in the channel region of our blend transistors. Less than 1.6% [44] of the initially accumulated mobile charges induced by the gate bias can be trapped at only a few locations inside the channel (Fig. 6b). This explains why we do not observe threshold voltage shifts in our blend transistors. Whether and how much the trapped charges will mitigate charge transport in the channel cannot be determined or quantified. If any, it is expected to result in a decrease in channel conductivity, but in fact we observe the opposite. The net positive effect of polymer blending indicates that a complex interplay between different mechanisms is taking place here.

4. Conclusions

To conclude, we have presented a systematic study of the influence of material composition and ink-jet process-

ing conditions on the charge transport in bottom-gate field-effect transistors based on single droplets of TIPS-PEN/PS blends. Under optimal conditions the field-effect mobility of the blends is significantly higher than that of the pure TIPS-PEN. In addition, blending results in much better sub-threshold characteristics. These results represent an important step towards the application of ink-jet printing for controlled deposition of high-performance transistors in large-area organic electronics. Using channel scaling measurements and SKPM measurements, we show that the sharp turn-on in current in the blends is the result of a contact resistance that originates from a thin insulating PS layer between the injecting contacts and the semiconductor channel. This insight suggests that reducing the contact resistance is the best way forward to improve the transistor characteristics even further.

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